ECE 4310: Introduction to VLSI design

Credit / Contact hours: 3 / 3

Course coordinator: Dr. Tooraj Nikoubin

Textbook(s) and/or other required material: We are primarily using slides and some journal and conference papers. Following is the most important reference book in this course.

Digital Integrated Circuits (Second Edition), Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic

Catalog description: A basic introduction to very large-scale integrated design of circuits and devices. Geometrical patterns of semiconductor devices on a chip, MOS circuits, masking and patterning, and automation tools.

Pre-requisite(s): 2.5 TTU GPA; C or better in ECE 3312

Co-requisites (if any): None

Designation: Required

Course learning outcomes: Upon completion of this course, students should be able to do the following:

- Analysis, Design and Optimization of Digital VLSI circuits in Gate level, Transistor Level and Layout Level in CMOS technology,
- Design with different logic styles like C-CMOS, PTL, CPL, DCVS, CDM
- Understanding physical aspects of the VLSI circuits design which drive energy, delay, area, and noise in digital circuits.
- Arithmetic circuit design and optimization for VLSI circuits
- Use of standard CAD tools (Cadence, Hspice and Verilog) for full custom and semicustom design flow and test
- Standard cell library designs for CMOS and FinFET technologies
- Memory Cell design

ABET Student Outcomes addressed in course: b, e, j and k

Topics covered:

Topics	Lectures
• Introduction, Transistor, Fabrication and Layout	3L
• CMOS Logic Design styles I	3L
• Logical effort transistor sizing and analysis	2L
• Current Mode circuits and MVL logic	1L
• Memories and PLAs	2L
• Project guide (Hspice, Cadence, Verilog)	1L
• Design and optimization of Arithmetic circuits I	2L
• Design and optimization of Arithmetic circuits II	2L
• CMOS Logic Design Styles II	1L
• Noise analysis and Delay modeling of CMOS circuits	1L
• Iterative Solution for Sizing, Sizing for Minimum Delay, Power or PDP	1L
• Project guide (Hspice, Cadence, Verilog)	1L
• Faults, Testing & Test Generation	1L
• Low Power CMOS Logic Circuits, Emerging Technologies	2L
• Circuit Pitfalls, Chip input and output (I/O) circuits	2L
• Review, Midterm and Final Exams	3L
Total	28L

L=75 Min